

## EECC 341 – Introduction to Digital Systems, Spring 2009

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### **Instructor:**

Shanchieh Jay Yang, [jay.yang@rit.edu](mailto:jay.yang@rit.edu), <http://www.ce.rit.edu/people/yang>  
Office Hours: Please refer to my homepage (My schedule is shown at the bottom.)

### **Description:**

The course covers the specification, analysis and design of digital systems. This includes the study of combinational and sequential systems using standard modules such as decoders, encoders, multiplexers, shifters, adders, registers and counters. The laboratory provides more insight into the physical and circuit aspects of the design and implementation of digital systems using SSI, MSI and LSI components as well as CAD tools.

### **Meeting Times and Rooms:**

- Lectures: MWF 1200-1250am (09-2139)
- Laboratories: Students may be in different lab sessions.

### **Online Access:**

- Homework assignments: <http://www.ce.rit.edu/people/yang/0306-341>
- Reference materials: [http://www.ce.rit.edu/studentresources/reference\\_materials/341/](http://www.ce.rit.edu/studentresources/reference_materials/341/)
- Mycourses access: <http://mycourses.rit.edu>

**Note: Class notes and homework assignments are posted online for students to download. Students are responsible to observe announcements sent via Email addresses used in <http://mycourses.rit.edu> and the SIS system.**

### **Textbook and Materials:**

- Fundamentals of Logic Design, Charles H. Roth, Jr., Brooks/Cole Thompson Learning.
- RIT CE Digital Systems Laboratory Manual & Lab. Kit (You may go pay and obtain receipt from the campus computer store - Digital Den next to SAU. The receipt will be used to exchange for the manual and lab kit in the first week of lab.)

### **Grading Policy:**

- Final Exam: 30%
- Midterm: 20% (TBD – either April 10, 13, or 15.)
- Quizzes: 10%
- Labs: 30%
- Homework: 10% (Lowest hw grade will be dropped)

**Note that no late homework or make-up quizzes or exams will be accepted. All special arrangements need to be made with 24-hour advance notice to the instructor.**

**Tentative Lecture Schedule:**

<b>Topic</b>	<b>Lectures</b>	<b>Sections</b>	<b>Labs</b>
Introduction: Digital Logic and Binary Numbers	1	1.1-1.2	Lab kits, accounts, rules, reports
Circuits and electronic components for digital logic	1	App.A, Lab Manual	
Boolean Algebra	2	Ch.2, Ch.3	Digital input / output
Minterm, Maxterm, Combinational Circuit Analysis	2	Ch.4	
Combinational Circuit Design	4	Ch.5, Ch.7, Ch.8	Logic gate charac. (e.g., AND)
Numbering Systems / Binary Arithmetic Operations	2	1.3, 1.4	K-map (Parking Lot, etc)
Arithmetic Units: Comparators, Adder, Subtractor	1	Notes, Lab manual	
Decoder, Encoder, Multiplexer, Demultiplexer	3	Ch.9, Lab Manual	Decoder/Multiplexer
Sequential Circuit: Latches and Flip-flops	3	Ch.11	Adder/Subtractor
Counters and Shift Registers	2	Ch.12	Ring Counter, Shift Register
Synchronous Sequential Circuit Analysis	3	Ch.13, Ch.14	Serial Adder/Subtractor
Synchronous Sequential Circuit Design	3	Ch.16	

**Note:** The online notes shall serve as the summary for your study. Not all of the material in the online notes will be covered. The textbook has a study guide and sample exercises at the beginning and at the end of each chapter. It is highly recommended that student should use both the textbook and online notes for study. A mentoring lab is in place to help students on both math courses and this course. Please refer to the KGC OE homepage for the freshman mentoring lab schedule. Students are highly encouraged to talk to the instructor early to ensure they are on the right track for the course.