Research Challenges in High Performance VLSI Circuits

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Agenda

- Fundamental trends in high speed, high complexity systems
- Current research problems and challenges
- Recent research results
- Conclusions
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Design Goals of CMOS Integrated Circuits

- **1970's**: Area
- **1980's**: Speed/Area
- **1990's**: Speed/Power
- **2000's**: Speed/Power/Noise

- **Ultra-Low Power**
High Performance Digital IC Design Challenges

• Primary objectives
  - Improve chip functionality
  - Improve circuit density
  - Improve performance

  More transistors  Smaller transistors  Faster transistors

  Larger ICs  On-chip scaling  Higher clock speeds

Design complexity  Noise sensitivity  Power dissipation

Interconnect design  Synchronization  Low power design
IC Design Gap

- Semiconductor manufacturing capability outpaces design productivity

- Design gap in *growth per year*
  - Density → 58%
  - Utilization → 21%

SRC PDTF Report 1997
Sources of Uncertainty

• Design Uncertainty
  – Lack of design details
  – Changes in specification

• Model Uncertainty
  – Model accuracy
  – Conservative models

• Process Uncertainty
  – Manufacturing imperfections
  – Changes in technology

Importance of Interconnect

- With technology scaling
  - Gate delay decreases
  - Wire length increases
  - Wire cross sectional area decreases
- Wire delay increases polynomially with technology scaling
History of Interconnect Modeling

- Gate delay was dominant
  - Interconnect was modeled as short-circuit

- Interconnect capacitance became comparable to gate capacitance

- Interconnect resistance became comparable to gate resistance
Modeling Interconnect Inductance

- Factors that make inductance effects important
  - Signal transition times are much shorter
    - Comparable to the signal time of flight
    - Faster devices
  - Reduction in interconnect resistance
    - Wide lines at higher metal layers
    - Introduction of low resistance materials for interconnect

\[
\begin{align*}
C_{\text{line}} &= Cl \\
R_{\text{line}} &= Rl \\
L_{\text{line}} &= Ll
\end{align*}
\]
Low Power Design Issues

- Power depends quadratically on $V_{DD}$
  - $V_{DD}$ scaling degrades speed
- Leakage current has become significant
  - Stand by power dissipation

Microprocessor Power Trend

- Total Power (watts)
- Year: 1998 to 2010
- Power trend shows an increase over time.
System Synchronization Styles

• Synchronization
  – Controls the flow of events within a system
  – All systems are asynchronous in reality
  – Provides an absolute or relative time reference
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Visible Current research problems and challenges
  - Signal Integrity
  - Interconnect design
  - Low power, high speed circuits
  - Global power distribution networks
  - Clock distribution network

- Recent research results

- Conclusions
Noise in Digital Integrated Circuits

- Traditional Definition of Noise
  - Undesired or unwanted energy
  - Degrades signal quality

- Voltage or current variations

- Temporal variations
  - Signal source
    - Clock jitter

- Delay uncertainty
  - Variations in signal delay propagation

\[ V_1 \quad \Delta V \quad V_2 \]

\[ \Delta t \]

\[ \text{Signal Propagation} \quad \Delta t \quad \text{Target Delay} \]
Interconnect Capacitive Coupling

- Fringing capacitance increases with scaling
  - Spacing between lines decreases
  - Capacitive voltage divider creates coupling
    - Produces variation in the signal delay
Capacitive Coupling Noise

• Signal Coupling
  – Crosstalk
  – Aggressor – victim model
    • Aggressor: line generating noise
    • Victim: noise sensitive line

• Variations in signal delay
  – Simultaneous switching noise
  – Variations in effective coupling capacitance

*K. T. Tang and E. G. Friedman.,” Delay and Noise Estimation of CMOS Logic Gates Driving Coupled Resistive-Capacitive Interconnections,” Integration, the VLSI Journal, September 2000
Inductive Coupling

- **On-chip inductance effects**
  - Increasing importance
    - Faster edge rates
    - Longer interconnect lengths on-chip
  - Mutual inductive coupling
    - Strongly depends upon the current return path
    - Return path can vary dynamically
Dependence of Inductance on Frequency

• Skin Effect
  – Low frequency
    • Current flow is uniformly distributed within the wire
  – High frequency
    • Current flow concentrates at the wire surface

• Proximity effect
  – No effect at low frequency
  – High frequency
    • Return current concentrates along the edges
Interconnect Shielding

• Insert power lines among signal lines
  – Isolates an aggressor (noisy) line from sensitive neighboring lines
  – Increases the noise tolerance of a sensitive line

• Reduces capacitive coupling
  – The voltage of the shield lines typically does not switch
  – Reduces variations of the effective line capacitance
    • Reduced delay uncertainty

• Controls mutual inductance effects
  – The current return path is clearly determined
Shielding Efficiency

• Achieves a target reduction in noise
  – Uses minimal metal line resources

• Shielding close to the driver may be redundant
  – When crosstalk occurs farther from the wire driver
  – Peak noise increases

• Shielding line density
  – Tradeoff between
    • Noise reduction
    • Wire routing area

Other Noise Reduction Techniques

• Increasing wire spacing
  – Effective for capacitive coupling
  – Non-efficient use of routing area

• Improving circuit tolerance to noise
  – PseudoCMOS domino
    • CMOS noise margin
    • Domino switching speed
      – Use of keepers

Research Objectives

- Develop accurate models to characterize noise
- Develop efficient shielding methodologies
- Enhance circuit tolerance to noise
- Exploit on-chip inductance for low power
- Improve CAD tools for on-chip inductance extraction
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Aluminum vs Copper Characteristics

- **Aluminum lines**
  - Larger coupling capacitance
  - Larger coupling noise

- **Copper lines**
  - Lower resistance
  - Inductance effects are more significant in wider lines

Geometric Wire Characteristics

- **Narrow lines**
  - RC dominant
  - Quadratic delay with line length

- **Wide lines**
  - Less noise at the far end
  - Delay is linearly dependent on line length
  - Inductive behavior

Figures of Merit to Characterize On-Chip Inductance

- Compare a distributed $RLC$ model to a distributed $RC$ model

- $RC$ model is sufficient if:
  - Attenuation is sufficient large to make reflections negligible
  - Waveform transition is slower than twice the time of flight

\[
\frac{RL}{2} \sqrt{\frac{C}{L}} > 1
\]

\[
t_r > 2l\sqrt{LC} = 2T_O
\]

Interconnect Design

- Simultaneous driver and wire sizing
  - Optimize
    - Delay
    - Signal transition time
    - Dynamic and short circuit power

- Repeater insertion
  - Linear delay with wire length
  - Tapering factor - buffers
  - Optimal repeater sizing and spacing

- Active regenerators - boosters
  - Support bi-directional wire behavior
  - No spacing constraints
  - High power dissipation
Research Objectives

• Develop methodologies to characterize interconnect impedances

• Co-design interconnect drivers with wires
  – Optimize
    • Signal delay
    • Signal transition time
    • Reduction in power dissipation
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Low Power High Speed CMOS Circuits

- Power depends quadratically on $V_{DD}$
- Reduction in supply voltage
  - Degrades circuit speed

Microprocessor Power Trend

- Total Power (watts)
- Year
Leakage Current

• Leakage current is the primary source of power consumption in an idle circuit
• Sub-threshold current increases with scaling $V_{TH}$
• Assuming Moore’s law is obeyed in the future
  – Transistor count and microprocessor frequency doubles every two years
  – Aggressive threshold voltage scaling

• Leakage power is expected to exceed dynamic power in the near future
• Leakage reduction techniques are therefore necessary

Microprocessor power trend

Leakage Current Reduction

• Increase threshold voltage
  – Degrades circuit speed

• Dual $V_{TH}$
  – Domino Circuits

• High $V_{TH}$ for non-critical circuits
  – Reduced leakage current

• Low $V_{TH}$ for critical circuits
  – Increased speed

• Variable voltage threshold
• Adaptive body biasing
Multiple On-Chip Voltage Supply

• Multiple $V_{DD}$ microprocessors
  – Use low $V_{DD}$ on the critical circuits
    • Satisfy the circuit performance requirements
  – Use high $V_{DD}$ on the non-critical circuits
    • Maintain dynamic switching power within acceptable limits

• Multiple on-chip power supply sources
  – DC-DC voltage conversion circuits
  – Voltage interface circuits
  – Efficiency issues
    • Voltage conversion losses
Low Swing Interconnect

- Interconnect related power
  - 50% to 90% of the total power consumption
  - Lowers the signal voltage swing

- Voltage level converters
  - Driver end
    - Reduce the voltage swing
  - Receiver end
    - Regenerate high voltage level required by the circuit blocks
Research Objectives

• Investigate tradeoffs among
  – Power reduction
  – Cost and complexity increase in the manufacturing process
  – Degradation of signal characteristics
    • Delay
    • Transition time

• Reduce leakage current
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The Problem of Power Delivery

- **Objective:** Deliver power to the load while maintaining the power supply voltages within target noise margins under specified load demands

\[ V = V_{dd} - IR_p - L_p \frac{dI}{dt} \]

- **Obstacles:** Power lines are not ideal and have finite resistance and inductance
  - Resistive noise \( V_R = IR \)
    - Caused by high transient currents drawn by the load
  - Inductive noise \( V_L = L \frac{di}{dt} \)
    - Caused by high current slew rates \( di/dt \) produced by the load
Current Demands of Future Circuits

- Current slew rate demands are rising faster than average current demands
Design Issues in Power Distribution Networks

• Noise - voltage supply fluctuation
  – Resistance of the power supply lines
    • IR drop
  – Inductance effects
    • \( L \cdot \frac{dI}{dt} \) noise
  – Power grid resonance
    • Ringing effects

• Electromigration
  – Increased current density

• Network architecture
  – Resources allocation
  – Metal area optimization

• Heat dissipation
  – Temperature variations produce delay uncertainty
Design of Power Distribution Grids is a Multifaceted Problem

- $R$, $IR$, $J$, $L$, $Area$, $L \frac{di}{dt}$, grid architectures, decoupling capacitors, electromigration

Inductive Characteristics of Power Distribution Networks

• Affects the integrity of the signals
  – Primary current return path in on-chip single ended signals
  – Return current flows through neighboring signal wires
    • Causes signal-to-signal crosstalk

• Affects the integrity of the power supply
  – Simultaneous switching noise
  – $RLC$ resonances within the power grids
Resource Requirements for On-Chip Power Distribution

- Power distribution networks use an increasingly larger share of on-chip resources to meet increasing demands
  - Share of metal resources increases
    - IBM Power4 CPU: 28% of on-chip metal
    - Hewlett-Packard PA-8500: >35% of on-chip metal

- On-chip decoupling capacitors occupy significant area
  - Typically 5% to 15% of chip area

- Optimizing the on-chip power distribution network can significantly increase the share of metal resources available for signal routing
Research Objectives

- Explore inductive/resistance/area tradeoffs in on-chip power distribution grids
- Minimize resources used by power distribution networks
- Efficiently estimate inductance of the on-chip power grid
- Develop techniques to minimize power grid inductance
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Design Issues in High Performance Clock Distribution Networks

• Improve circuit performance
  – Increase clock frequency

• Relax tight timing constraints
  – Control the clock signal delay
  – Prevent variation of the clock signal from the target values
    • Delay uncertainty

• Reduce the power dissipated by the clock distribution network
  – Up to 70% of the total on-chip dynamic power*

Enhancing Circuit Performance

• Non-zero clock skew scheduling
  – Exploit the difference between data path delays
  – Reduce clock period

• Retiming
  – Re-position memory elements (registers) to minimize:
    • Clock period
    • Number of registers

• Wave pipelining
  – Propagate multiple data waves within the same clock period
  – Guarantee no interference among subsequent waves

*X. Liu, M. C. Papaefthymiou, and E. G. Friedman “Retiming and Clock Scheduling for Digital Circuit Optimization,” IEEE Tran. on CAD, Feb. 2002*
Controlling Clock Signal Variations

• Increasing clock frequencies
  – Tighter timing constraints

• On-chip feature size scaling aggravates delay uncertainty
  – Increased sensitivity to signal delay deviations

• Improve signal integrity
  – Clock buffer insertion
    • Increased power dissipation
    • May increase clock signal delay
  – Shielding of clock lines
    • Routing area limitations
    • Shielding efficiency
Research Objectives

• Control the variations of the clock signal delay
  – Enhance clock signal integrity
  – Satisfy timing constraints
  – Apply design strategies to improve performance
    • Non-zero clock skew
    • Retiming

• Reduce power dissipated by the clock distribution network
  – Develop efficient clock gating strategies
  – Design clock distribution network for minimum power
    • Repeater sizing and insertion
    • Wire sizing
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Recent research results
- Design methodologies for on-chip inductive interconnect
- Low power, high speed circuit design techniques
- On-chip DC-to-DC conversion
- Inductive characteristics of power distribution grids
- Reduced delay uncertainty in clock distribution networks
- Substrate coupling in mixed-signal integrated circuits

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Transient Power Tradeoff in Inductive Interconnect

- **Dynamic power** increases with line width
- **Short-circuit power** may decrease in underdamped highly inductive lines
- An optimum interconnect width exists
  - Minimum **transient power**

Transition Time Characteristics

- The characteristic impedance of the line decreases with increasing width
- Driving condition
  - Resistive
  - Overdriven
  - Matched
  - Underdriven

- Minimum transition time for line matched with the driver

An optimum width for minimum power exists.
Simultaneous Driver and Wire Sizing

• Larger driver reduces the signal transition time
  – Reduce short circuit power

• Analytical solution illustrates the minimum power
  – Specific driver and wire size that minimizes transient power

• Tradeoff between dynamic and short-circuit power in inductive interconnect
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Effects of On-Chip Interconnect Inductance on Circuit Design Methodologies

• Optimum sizing of $RLC$ line with repeaters
A tradeoff exists between
- Minimum signal propagation delay
- The total power dissipation in a repeater system driving an $RLC$ line
### Optimization Criteria for Interconnect Width

<table>
<thead>
<tr>
<th>$l = 5 \text{ mm}$</th>
<th>Minimum Power</th>
<th>No Repeaters</th>
<th>Minimum PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_{\text{int}}$ (μm)</td>
<td>0.8</td>
<td>2.1</td>
<td>2.1</td>
</tr>
<tr>
<td>Number of Repeaters</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Repeater Size</td>
<td>43.3</td>
<td>61.2</td>
<td>61.2</td>
</tr>
<tr>
<td>Min. Delay (nsec)</td>
<td>Total</td>
<td>0.157</td>
<td>0.051</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>Total</td>
<td>1.73</td>
<td>1.98</td>
</tr>
<tr>
<td></td>
<td>Increase</td>
<td>208%</td>
<td>0%</td>
</tr>
<tr>
<td></td>
<td>Increase</td>
<td>0%</td>
<td>14.5%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$l = 15 \text{ mm}$</th>
<th>Minimum Power</th>
<th>No Repeaters</th>
<th>Minimum PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_{\text{int}}$ (μm)</td>
<td>0.8</td>
<td>20</td>
<td>3.9</td>
</tr>
<tr>
<td>Number of Repeaters</td>
<td>5</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Repeater Size</td>
<td>43.2</td>
<td>225</td>
<td>80.7</td>
</tr>
<tr>
<td>Min. Delay (nsec)</td>
<td>Total</td>
<td>3.87</td>
<td>0.19</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>Total</td>
<td>5.2</td>
<td>21.31</td>
</tr>
<tr>
<td></td>
<td>Increase</td>
<td>1936%</td>
<td>0%</td>
</tr>
<tr>
<td></td>
<td>Increase</td>
<td>0%</td>
<td>310%</td>
</tr>
</tbody>
</table>

- For long lines, PDP is an effective criterion
  - Satisfies both high performance and low power requirements

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• Conclusions
Optimum Shaping of a Distributed \textit{RLC} Interconnect

- Line inductance increases the effectiveness of optimum wire shaping
  - Increased circuit speed
  - Reduced power dissipation
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  Recent research results
  – Design methodologies for on-chip inductive interconnect
  – Low power, high speed circuit design techniques
    – Low swing interconnect
    – Low leakage domino logic
    – Variable threshold voltage keeper
  – On-chip DC-to-DC conversion
  – Inductive characteristics of power distribution grids
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• Conclusions
Low Swing Interconnect

- Low power techniques
  - Reduce the supply voltage → Reduced circuit speed
    - Different blocks operate at different voltage levels
    - For signal transfer, specialized voltage interface circuits are necessary
  - Reduce the signal voltage swing on long interconnects

- Voltage level converters
  - Driver end
    - Reduce the voltage swing
  - Receiver end
    - Regenerate high voltage level required by the circuit blocks
CMOS Voltage Interface Circuit

- Bi-directional full voltage level conversion
  - Driver end
    - High swing to low swing
  - Receiver end
    - Low swing to high swing

- No static DC currents
- High energy efficiency
  - 89% to 99% level conversion efficiency
    - Load range: 1 pF → 15 pF

Results of Circuit Analysis

• Lower power
• Enhanced performance
• Small area as compared to previously published circuits
  – Up to 3.6x delay improvement
  – Up to 198x power reduction

• 0.18 µm CMOS
• $V_{DD1} = 1.8$ volts
• $V_{DD2} = 3.3$ volts

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Area (normalized)</th>
<th>MFSO (MHz)</th>
<th>Power (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SF</td>
<td>2.8</td>
<td>240</td>
<td>4.5</td>
</tr>
<tr>
<td>CQ</td>
<td>2.1</td>
<td>200</td>
<td>17.8</td>
</tr>
<tr>
<td>ZGR</td>
<td>1.6</td>
<td>590</td>
<td>257.1</td>
</tr>
<tr>
<td>NIITA</td>
<td>1.0</td>
<td>380</td>
<td>2.9</td>
</tr>
<tr>
<td>KSF</td>
<td>1.3</td>
<td>610</td>
<td>1.3</td>
</tr>
</tbody>
</table>

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Leakage Current Reduction Technique

- A circuit technique* is proposed for reduced standby mode energy dissipation
  - Power, delay, and area efficient as compared to previously proposed schemes

- Proposed dual-$V_t$ domino circuit technique has significantly reduced leakage current as compared to a purely low-$V_t$ implementation
  - High-$V_t$ transistors are strongly cutoff

<table>
<thead>
<tr>
<th>Leakage Power</th>
<th>Standard</th>
<th>LS-Full</th>
<th>LS-Weak</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-$V_t$</td>
<td>249</td>
<td>238</td>
<td>235</td>
</tr>
<tr>
<td>Dual-$V_t$</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>High-$V_t$</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Standard: standard domino logic circuit, LS-Full: low swing domino with a full swing keeper, LS-Weak: low swing domino with a low swing keeper

Domino Logic Characteristics

- **Reduced $V_T$**
  - Enhanced speed
  - Low supply voltage
  - Low noise immunity

- **Low swing domino logic is proposed**
  - Reduced dynamic power consumption
  - No noise immunity degradation

Simulation Results

- Fully driven keeper circuit
  - Enhanced power
  - Enhanced noise immunity
    - As compared to standard domino

- Weakly driven keeper circuit
  - Reduced contention current
  - Reduced power
  - Enhanced speed
    - As compared to fully driven domino

<table>
<thead>
<tr>
<th></th>
<th>Power</th>
<th>Delay</th>
<th>MTNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard domino</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>Fully driven keeper</td>
<td>0.91</td>
<td>1.46</td>
<td>1.03</td>
</tr>
<tr>
<td>Weakly driven keeper</td>
<td>0.88</td>
<td>1.38</td>
<td>0.98</td>
</tr>
</tbody>
</table>

MTNA: Maximum tolerable noise amplitude
**Dual $V_T$ Domino Logic**

- Enhance the proposed low swing domino circuits
  - Reduced standby leakage current
    - High $V_T$ transistors are strongly cut-off in the standby mode

- Proposed dual-$V_T$ circuit technique reduces
  - Standby mode leakage (~235 times)
  - Active mode total power
  - Evaluation delay
    - As compared to low-$V_T$ circuit

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Variable Threshold Voltage Keeper

- Precharge phase
  - Keeper is reverse body biased

Variable Threshold Voltage Keeper

- **Precharge phase**
  - Keeper is reverse body biased
- **Evaluation phase**
  - Keeper has a high-$V_t$
    - Reduced contention current
    - Enhanced speed and power characteristics

Variable Threshold Voltage Keeper

- **Precharge phase**
  - Keeper is reverse body biased

- **Evaluation phase**
  - Keeper has a high-$V_t$
    - Reduced contention current
    - Enhanced speed and power characteristics
  - Keeper is zero body biased after a delay $t_D$
    - Enhanced noise immunity

Delay, Power, and NML Characteristics

- Domino logic with variable threshold voltage keeper
  - Up to 60% improved delay
  - 37% reduced power dissipation
  - 75% lower power delay product (PDP)
  - Temporary degradation of noise margin by 15%
    - Only at the beginning of the evaluation phase
- Effectiveness of the technique is enhanced with increased keeper width

SD: standard domino
DVTVK: domino logic with a variable threshold voltage keeper
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High-Efficiency Monolithic DC-DC Converters for Dual-$V_{DD}$ Microprocessors

- Advantages of integrating the DC-DC converter with the microprocessor
  - Reduced parasitic losses higher efficiency
  - Lower fabrication cost
- High switching frequency reduces the size of the passive devices
- A monolithic high-efficiency DC-DC converter can be realized utilizing a high switching frequency in the GHz range
- Efficiency characteristics of a buck converter change dramatically with increased switching frequency
  - Reduced inductance and capacitance has lowered parasitic losses
  - Complicated tradeoffs exist among inductor and MOSFET-related switching and conduction losses
Switching DC-DC Converters

- Switching DC-DC converters have high efficiency characteristics
- Sources of energy loss
  - Wiring between the passive and active devices inside the converter
  - Wiring from the DC-DC converter output to the microprocessor input pads
Model of a Monolithic Buck Converter

• A parasitic model of a buck converter has been developed
• A closed form expression that characterizes the power dissipation of a buck converter is proposed

• An optimum switching frequency and inductor current ripple pair exists that maximizes efficiency
  – 92% maximum efficiency
  – \( f_s = 114 \text{ MHz}, \Delta i = 9.5 \text{ A} \)
  – \( L = 104\text{pH}, C = 2.1 \mu\text{F} \)

• A design space that permits full integration of an on-chip DC-DC converter has been determined

Analysis with Limited Filter Capacitance

- Area overhead of an integrated filter capacitor
- Maximum achievable efficiency is reduced with decreased filter capacitance
  - $L$ and $f_s$ both increase
    - Increased energy dissipation

<table>
<thead>
<tr>
<th>$C$ (nF)</th>
<th>$\eta$ (%)</th>
<th>$f_s$ (MHz)</th>
<th>$L$ (pH)</th>
<th>$W_{P1}$ (mm)</th>
<th>$W_{N1}$ (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>74.7</td>
<td>3174</td>
<td>279</td>
<td>51</td>
<td>20</td>
</tr>
<tr>
<td>10</td>
<td>82.8</td>
<td>1227</td>
<td>187</td>
<td>82</td>
<td>33</td>
</tr>
<tr>
<td>100</td>
<td>88.4</td>
<td>477</td>
<td>124</td>
<td>132</td>
<td>53</td>
</tr>
</tbody>
</table>

80 nm CMOS technology, $V_{DD1} = 1.2$ volts, $V_{DD2} = 0.9$ volts, $\eta$: efficiency, $f_s$: switching frequency, $C$: filter capacitance, $L$: filter inductance, $W_{P1}$: width of the power PMOS $P1$, $W_{N1}$: width of the power NMOS $N1$

- 86% efficiency determined by simulation
  - Within 2.4% of our model

Agenda

• Fundamental trends in high speed - high complexity systems

• Current research problems and challenges

☞ Recent research results
  – Design methodologies for on-chip inductive interconnect
  – Low power, high speed circuit design techniques
  – On-chip DC-to-DC conversion
  – Inductive characteristics of power distribution grids
  – Reduced delay uncertainty in clock distribution networks
  – Substrate coupling in mixed-signal integrated circuits

• Conclusions
Impedance Characteristics of Multi-Layer Power Distribution Grids

- Complex structures containing multiple conductors with different electrical characteristics
  - Grid resistance and inductance vary with frequency
• Global power distribution networks are conservatively designed to meet worst case requirements
Dependence of Inductance on Frequency: Skin and Proximity Effects

• Inductance of a conductor decreases with frequency due to several effects
  – Although inductive impedance $j\omega L$ increases with frequency $f$

• Skin effect
  – Current concentrates at the surface of a conductor
  – Internal inductance of the conductor decreases
    • Current and magnetic field at the core of the conductor decrease
  – Negligible effect on inductance in integrated circuits
    • The drop in the internal inductance is negligibly small
      – A fraction of the low frequency internal inductance, 0.05 nH/mm

• Proximity effect
  – Current concentrates on the conductor side closest to the current return path
  – Significant only in adjacent wide wires carrying very high frequency signals
Dependence of Inductance on Frequency: Multi-path Current Redistribution

- In a circuit with multiple current paths the distribution of the current flow is frequency dependent
  - Low frequency — determined by the resistance of the paths
  - High frequency — determined by the inductance of the paths

\[ I_1 \approx I_0 \frac{R_2}{R_1 + R_2} \quad I_2 \approx I_0 \frac{R_1}{R_1 + R_2} \]

- This effect is the primary source of inductance variation with frequency in integrated circuits
Grid Layers Typically Have Disparate Electrical Characteristics

- Grid layers have different resistive and inductive characteristics
  - Layers with smaller net cross-sectional area have higher resistance
  - Layers with smaller line pitch have lower inductance
  - Lower grid layers have smaller line width, height, and pitch
    - Lower inductance and higher resistance
- Each layer can be modeled as a separate $RL$ branch
Impedance Characteristics of Individual Grid Layers

- Each layer serves as the lowest impedance path within a certain frequency range
  - Carries the largest share of current
  - Has the greatest impact on the overall impedance

\[ R_1 < R_2 < \cdots < R_N \]
\[ L_1 > L_2 > \cdots > L_N \]
Frequency Variation of Inductance and Resistance in Multi-Layer Grids

- Significant multi-path current redistribution
  - Low frequency inductance is determined by the upper layer
  \[ L = L_1 \left( \frac{R_2}{R_1 + R_2} \right)^2 + L_2 \left( \frac{R_1}{R_1 + R_2} \right)^2 \quad L_1 \gg L_2 \quad R_2 \gg R_1 \]
  - High frequency inductance is determined by the lower layer
  \[ L = \frac{L_1 L_2}{L_1 + L_2} \]
Conclusions

• Inductance and resistance of multi-layer grids vary significantly with frequency
  – Unlike the inductance and resistance of an individual grid layer
  – Due to disparate electrical properties of comprising grid layers
    • Significant current redistribution with frequency among grid layers
    • Grid inductance interacts with grid resistance
• An analytical model has been developed to determine the inductive and resistive characteristics of a multi-layer grid
  – Supports the efficient design of power distribution grids
    • Efficient design space exploration early in the design cycle
    • Efficient allocation of decoupling capacitance
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• Conclusions
Enhancing Clock Tree Topology

- Key Concept:
  - The larger the common part of the clock tree shared by the two signals that drive the sequential-adjacent registers
  - The smaller the delay uncertainty for the data path between these registers

- Approach:
  - Change the hierarchy of the branch nodes within the clock tree
    - Increase the common part of the clock paths driving the critical data paths
  - The delay uncertainty is shifted to less sensitive data paths

Data Path Tolerance to Delay Uncertainty

- Uncertainty graph
  - Describes the tolerance of the data paths to clock signal delay uncertainty

- Tolerance of a data path to delay uncertainty determines
  - Maximum number of non-common branch nodes between the clock paths that drive this path
• Delay uncertainty of the critical paths is either reduced or unchanged

• The delay uncertainty is increased in one non-critical path only
The reduction in delay uncertainty is determined for four different branching factors (BF)

- The smaller the branching factor
  - The deeper the clock tree
  - The greater the reduction in delay uncertainty
Demonstration of Layout Improvements

- Increase in total wire length in RDU: 4.5%

<table>
<thead>
<tr>
<th>Data Paths</th>
<th>Wire length of the non-common part of the clock tree</th>
<th>Delay Uncertainty between clock signal paths</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MWL tree</td>
<td>RDU tree</td>
</tr>
<tr>
<td>2 → 3</td>
<td>13.5</td>
<td>11.1</td>
</tr>
<tr>
<td>1 → 3</td>
<td>12.6</td>
<td>10.2</td>
</tr>
<tr>
<td>6 → 4</td>
<td>12.4</td>
<td>12.6</td>
</tr>
<tr>
<td>11 → 4</td>
<td>7.9</td>
<td>5.5</td>
</tr>
<tr>
<td>3 → 4</td>
<td>7.3</td>
<td>4.9</td>
</tr>
<tr>
<td>10 → 3</td>
<td>7.4</td>
<td>5.7</td>
</tr>
<tr>
<td>8 → 3</td>
<td>1.9</td>
<td>1.9</td>
</tr>
<tr>
<td>11 → 3</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>Average</td>
<td>7.9</td>
<td>6.5</td>
</tr>
</tbody>
</table>
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Substrate Coupling in Mixed-Signal Integrated Circuits

- Sources of coupling noise
- Digital switching noise can affect sensitive analog circuits
- High power analog circuits can affect digital circuits
- Store incorrect state in bistable register
Project Goals

• Enhance quality and decrease cost of ink jet printers

• Evaluate analog-to-digital substrate coupling
  – High current, high power analog devices can cause incorrect data to be latched into a bistable register

• Develop design techniques to mitigate substrate coupling effects
  – Ground line isolation
  – Substrate contact placement
  – Power driver circuit characteristics
    • Physical transistor size and drift region
  – Influence of circuit placement on noise
    • Directional effects
  – Quantitative estimation of noise
  – Parameter extraction for model development
Experimental Analysis and Evaluation

- Test circuits have been designed and fabricated
- Various parameters effecting coupling noise have been evaluated on experimental circuit tests

Feedback Behavior of Substrate Coupling

- Noise waveforms generated within the substrate by power drivers have been individually monitored.
- Power transistors are observed to generate noise during both switching and normal operation.

Experimental Analysis of Test Circuits

- Factors effecting the noise tolerance of static and dynamic registers have been evaluated
  - Clocking regime
  - Physical separation
  - Driver power supply voltage
  - Number of active drivers
  - On-chip location

![Graph showing noise level vs. active drivers (3-7)](image)

![Graph showing noise level vs. clocking regime (1-4)](image)

![Graph showing noise received vs. physical separation (350 µm - 500 µm)](image)

![Graph showing noise tolerance vs. clocking regime (1-4)](image)
Substrate Contact Placement

- Careful substrate contact placement can
  - Minimize the amplitude of the substrate noise
  - Reduce the noise nonuniformity
- A methodology has been developed for placing substrate contacts to reduce noise

Epi technology

Non-epi technology

Substrate noise distribution

Agenda

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• Recent research results

❖ Conclusions
Conclusions

• Fundamental design issues and trends
  – Specific to high performance, high complexity VLSI based digital circuits

• Reviewed primary design bottlenecks in high performance CMOS circuits

• Discussed recent research results

• The quest never ends!
  – There are all kinds of exciting problems to work on as we move into the world of CMOS nanometer design