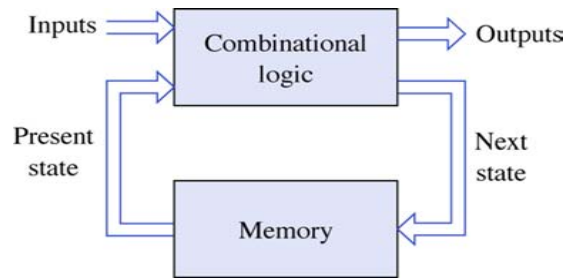


Topic #7 – Latches & Flipflops

Why sequential logic?

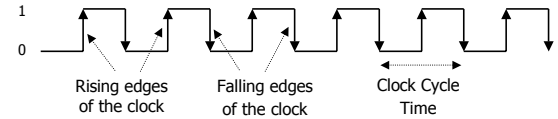
Maintain the notion of **state** (outputs of memory elements) that depends on **current inputs** and **past history of inputs**, and possibly triggered by **clock** signal.



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Clock & synchronous sequential circuit

Clock:



- Clock Frequency = $1 / \text{clock cycle time}$ (cycles per sec/Hz)
 - Ex: Clock cycle time = 1ms \Rightarrow frequency = 1000Hz

- **Synchronous Sequential Circuits:** state changes only when
 1. the clock value stay at 1 (or 0)
 2. the clock signal changes, i.e., at the rising (or falling) edges
- Asynchronous: data driven state transition ...

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Sequential circuit elements

Latches:

- output depends on its current inputs and current state (past inputs)
- state transition does not depend on clock
- S-R Latch
 - S-R Latch With Enable
 - D-Latch

Flip-Flop:

- output depends on its current inputs and current state (past inputs)
- state may only change when clock signal is in desired state
- D Flip-Flops
- J-K Flip-Flops
- T Flip-Flops

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Describing Sequential Circuits

State table

- For each current-state, specify next-states as function of inputs
- For each current-state, specify outputs as function of inputs

State diagram

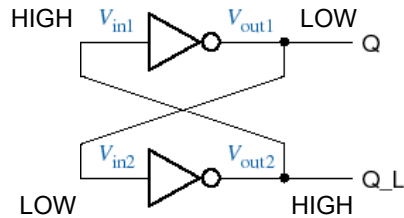
- Graphical version of state table

More on this later

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Bistable element

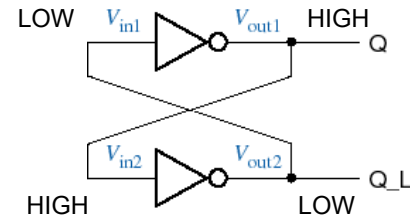
- The simplest sequential circuit
- Two states
 - One state variable, say, Q



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Bistable element

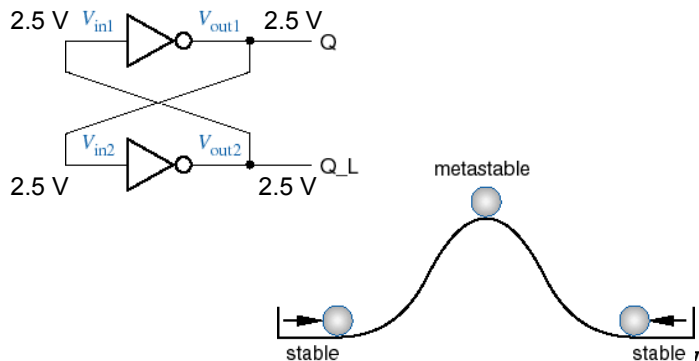
- The simplest sequential circuit
- Two states
 - One state variable, say, Q



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Metastability

- Metastability is inherent in any bistable circuit



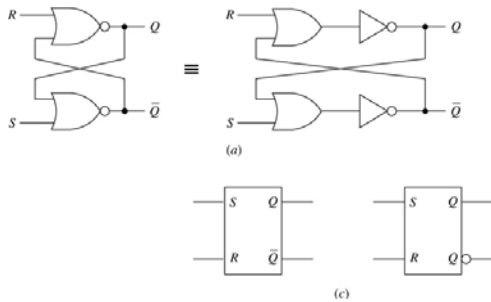
Why all the harping on metastability?

- All real systems are subject to it
 - Problems are caused by "asynchronous inputs" that do not meet flip-flop setup and hold times
 - Details in Chapter-7 flip-flop descriptions
 - Especially severe in high-speed systems
 - since clock periods are so short, "metastability resolution time" can be longer than one clock period
- Many digital designers, products, and companies have been burned by this phenomenon.

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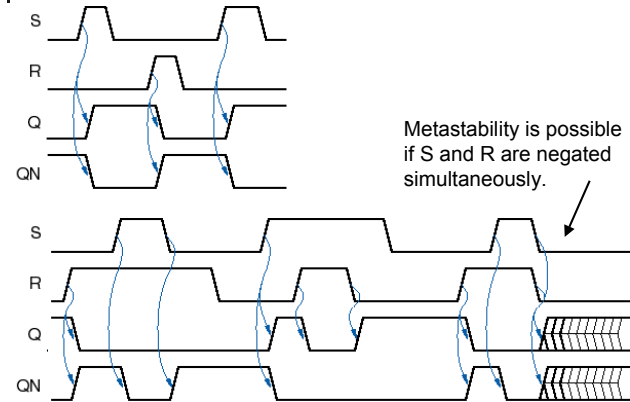
Controlling the bistable circuit

- Idea: use input to lock state
- S-R latch



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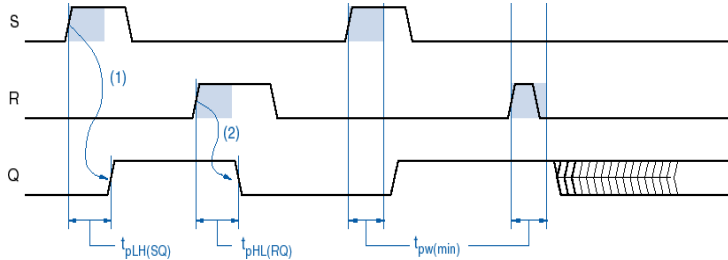
S-R latch operation



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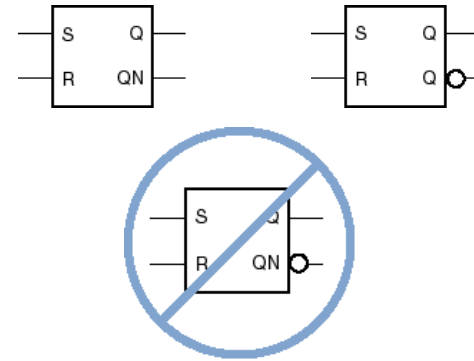
S-R latch timing parameters

- Propagation delay
- Minimum pulse width



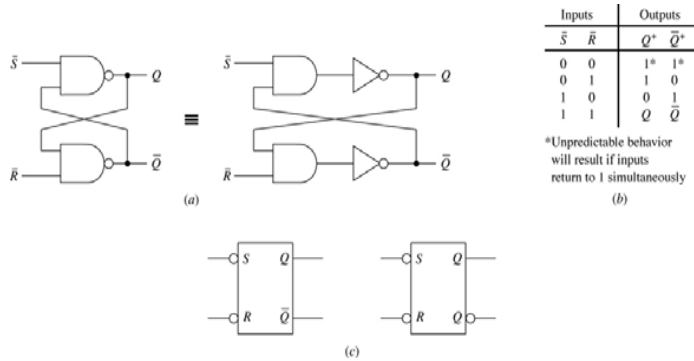
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S-R latch symbols



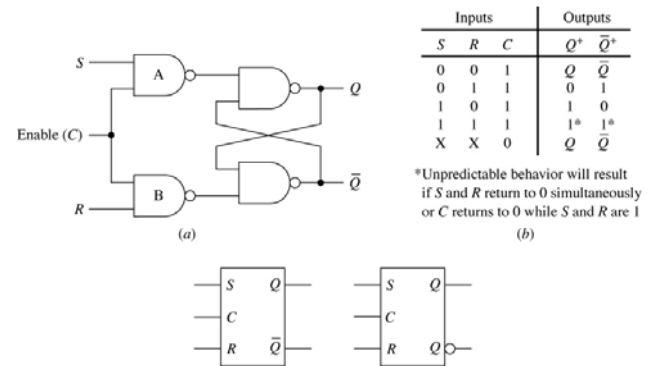
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S-R latch using NAND gates



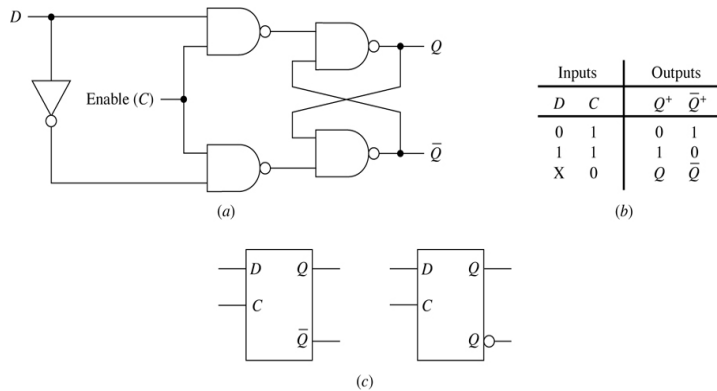
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S-R latch with enable (clock)



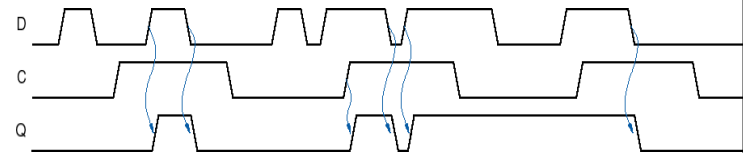
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D latch



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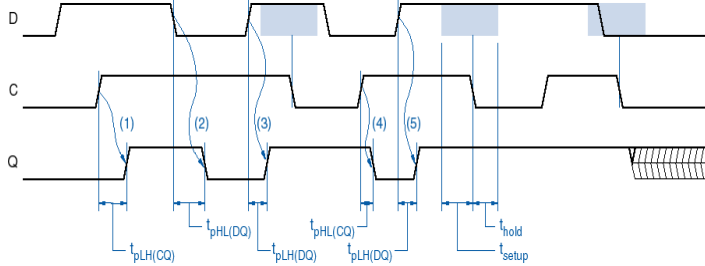
D-latch operation



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D-latch timing parameters

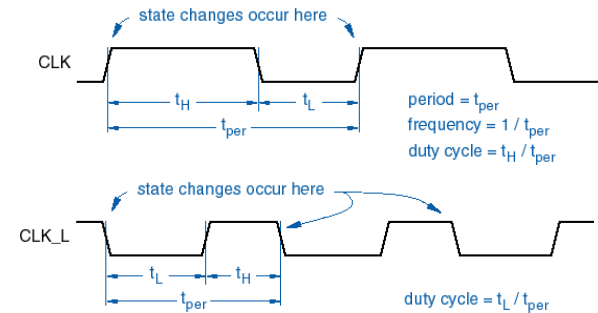
- Propagation delay (from C or D)
- Setup time (D before C edge)
- Hold time (D after C edge)



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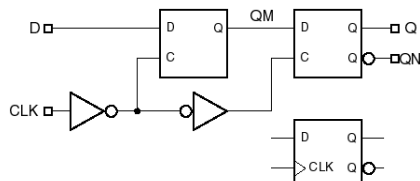
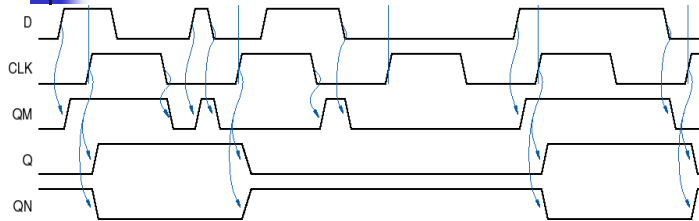
Level vs. edge triggered sequential circuit

- Clock signal revisited
 - Most sequential logic today trigger state change at clock edge.



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Edge-triggered D flip-flop behavior

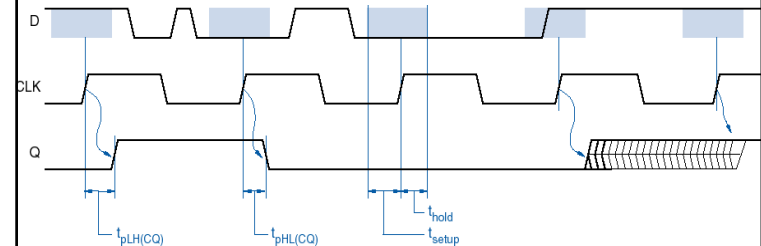


D	CLK	Q	QN
0	↓	0	1
1	↓	1	0
x	0	last Q	last QN
x	1	last Q	last QN

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D flip-flop timing parameters

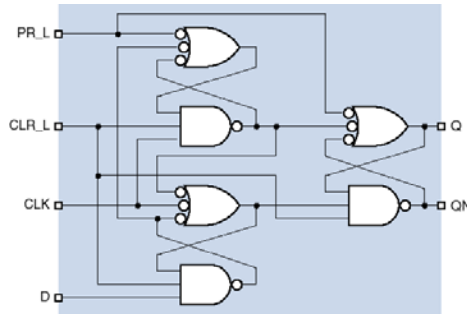
- Propagation delay (from CLK)
- Setup time (D before CLK)
- Hold time (D after CLK)



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TTL edge-triggered D circuit

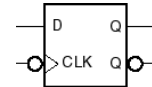
- Preset and clear inputs
 - like S-R latch
- 3 feedback loops
 - interesting analysis
- Light loading on D and C



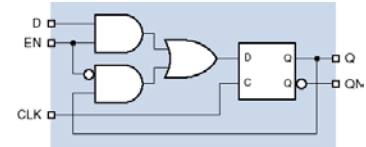
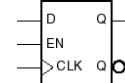
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Other D flip-flop variations

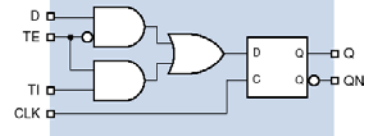
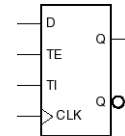
- Negative-edge triggered



- Clock enable

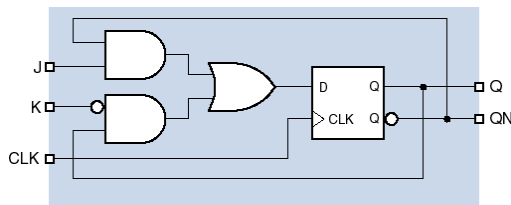


- Scan



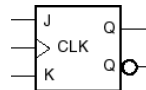
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J-K flip-flops



- Not used much anymore

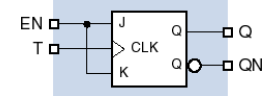
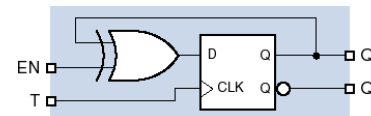
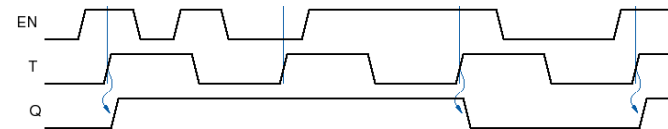
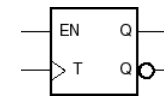
J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q



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T flip-flops

- Important for counters



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