

Exercise 4: Combinational Logic Circuit Design Using Karnaugh Map Simplification

Lab Component		Point Value	Points Earned	Comments
Signatures	<i>Prelab</i>	20		Part 1 Part 2
	<i>Demo</i>	40		
Abstract		3		
Design Methodology	<i>Discussion</i>	3		
	<i>Karnaugh Maps</i>	4		
	<i>Reduced SOP Expression</i>	3		
	<i>Reduced POS Expression</i>	3		
	<i>Schematic</i>	3		
Results and Analysis	<i>Discussion</i>	3		
Conclusion		3		
Questions	<i>Q1</i>	5		
	<i>Q2</i>	5		
	<i>Q3</i>	5		
TOTAL		100		