

EECC 0306-351-01

Hardware Description Languages

Spring 2004/2005

Instructor:

Marcin Lukowiak, mxleec@rit.edu, <http://www.ce.rit.edu/~lukowiak>

Office: 17-3625

Phone: (585) 475-2808

Course Description:

The course presents different approaches to the digital system description and design with the use of VHDL. The theory is exemplified by a lot of practical realization of the digital systems.

Computer usage is required to complete the course projects. UNIX(PC)-based VHDL tools are used in the development and simulation of the projects. The laboratory projects are organized in a series, which ensure that the topics of the course are fully understood as the course progresses. The projects include the whole design flow: design, simulation and synthesis. Mentor Graphics (ModelSim) and Synopsys are used as a computer tools to make the design.

Prerequisites:

0306-341 – Introduction to Digital Systems Design

Classes:

Monday : 9.00am - 9.50am 9-3139
Wednesday: 9.00am - 9.50am 9-3139
Friday : 9.00am - 9.50am 9-3139

Labs:

Tuesday : 2.00pm - 3.50pm 17-2520 (351-40)
Tuesday : 4.00pm - 5.50pm 17-2520 (351-41)

Office hours:

Monday : 10.00am - 11.00am
3.00pm - 4.00pm
Wednesday: 3.00pm - 4.00pm

Textbook and materials:

No text book is required.

On-line materials will be posted on instructor's web page (<http://www.ce.rit.edu/~lukowiak>) and <http://mycourses.rit.edu>.

Additional books:

- HDL Chip Design, Douglas J. Smith, Doone Publication, Ninth printing July 2001.
- VHDL Primer, J.Bhasker, Prentice Hall 1999.
- The Designer's Guide to VHDL – Second Edition, Peter J. Ashenden, Morgan Kaufmann Publishers 2002.
- Digital Design and Modeling with VHDL and Synthesis, K.C.Chang, IEEE Computer Society Press 1997.
- Introductory VHDL From Simulation to Synthesis, S. Yalamanchili, Prentice Hall 2000.
- Digital Systems Design using VHDL, Charles H.Roth, PWS 1998.
- Digital Systems Design with VHDL and Synthesis An Integrated Approach, K.C.Chang, IEEE Computer Society Press 1999.
- VHDL: Programming by Example – Fourth Edition, Douglas L. Perry, McGraw-Hill 2002.

Grade Weighting:

Labs/Homework	:	50%	(40% + 10%)
Quizzes	:	10%	
Midterm	:	15%	
Final Exam	:	25%	

Tentative Topics

	Class topics	Lab, homework
Week1	Course policy; VHDL overview. Types, Signals, Variables, Constants, concept of Entity-Architecture pair.	
Week2	Discrete Event Simulation. Behavioral, Data Flow, RTL and Structural description in VHDL.	Lab#1. Introduction to ModelSim environment. Waveform generator.
Week3	Concurrent Statements. Process, Sequential Statements.	Lab#2. Modeling of combinational circuits using concurrent and sequential statements.
Week4	Quizz#1. VHDL models for some basic digital circuits. The idea of a test bench and its implementation in VHDL.	Lab#3. Parallel Even-Parity Detector & The Fibonacci Series Generator.
Week5	Behavior and structural modeling of State Machines.	Lab#4. Serial Adder and its Testbench (array of records, assert statement).
Week6	Midterm Exam. Attributes, Generics, Configurations.	Lab#5. Finite State Machine – behavioral and structural description.
Week7	Basic Input/Output, Assert statement. Digital Systems Design Flow, Synthesis.	Lab#6. Combinational multiplier for unsigned binary numbers. Introduction to synthesis.
Week8	Introduction to Verilog HDL.	Continuation of Lab#6.
Week9	Quizz#2. Memories and buses. Tri-state buffers.	Lab#7. High level, behavioral description of a complex digital system for image processing. Synthesis of State Machines. Modeling of combinational circuits in Verilog.
Week10	Modeling of inertial and transport delays. Subprograms (procedures, functions – operators), Packages, and Libraries. Resolution function.	

No late reports or make-up quizzes/exams will be accepted. All special arrangements need to be made 24 hours in advance to the instructor.

Students are responsible to observe announcements sent via Email addresses used in <http://mycourses.rit.edu> and online grading/early alert system.